CLAIMS

The invention claimed is:

1. A circuit, comprising:

a power storage element to generate a DC output voltage from an input voltage;

an output sampler to generate a feedback signal from the output voltage;

an error amplifier to generate an error signal from the feedback signal;

a comparator to generate a pulse signal by comparing a ramp signal and a compared voltage, wherein one of the ramp signal and the compared voltage is generated from the error signal; and

a power switch to switch the power storage element on and off as controlled by the pulse signal,

wherein the pulse signal is generated such that, if the input voltage changes within a first range, a width of pulses of the pulse signal changes so as to maintain the output voltage substantially constant.

2. The circuit of claim 1, wherein

the power storage element is arranged in a configuration that is one of a buck, a boost, a cuk, a sepic and a zeta configuration.

3. The circuit of claim 1, wherein

the output sampler includes an impedance divider.

4. The circuit of claim 1, further comprising:

a ramp generator to generate the ramp signal from the error signal, and

wherein the compared voltage is a preset substantially constant voltage.

5. The circuit of claim 4, wherein

the comparator and the ramp generator are reset by the same clock signal.

6. A DC to DC converter, comprising:

a power storage element to generate a DC output voltage from an input voltage;

an error amplifier to generate an error signal from the output voltage;

a ramp generator to generate a ramp signal from the error signal;

a comparator to generate a pulse signal by comparing the ramp signal to a preset threshold voltage; and

a power switch to switch the power storage element on and off as controlled by the pulse signal.

7. The converter of claim 6, wherein

the power storage element is arranged in a configuration that is one of a buck, a boost, a cuk, a sepic and a zeta configuration.

8. The converter of claim 6, wherein

the comparator and the ramp generator are reset by the same clock signal.

9. The converter of claim 6, further comprising:

an output sampler to generate a feedback signal from the output voltage, and

wherein the error amplifier uses the feedback signal as representative of the output voltage.

10. The converter of claim 6, wherein

the ramp generator includes

a ramp capacitor, and

a ramp switch to charge the ramp capacitor in accordance with the error signal.

11. The converter of claim 10, wherein

the ramp generator further includes a reset switch to short the ramp capacitor.

12. The converter of claim 10, wherein

the ramp generator further includes a linear element to control charging of the ramp capacitor through the ramp switch.

13. The converter of claim 12, wherein

the linear element is a resistor.

14. A device comprising:

means for alternatingly charging and discharging a power storage element to generate a DC output voltage from an input voltage;

means for generating an error signal from the output voltage;

means for generating a ramp signal from the error signal;

means for comparing the ramp signal to a preset threshold voltage to generate a pulse signal; and

means for using the pulse signal to control the charging and discharging of the power storage element.

15. The device of claim 14, wherein

the means for generating the ramp signal includes means for charging a ramp capacitor in accordance with the error signal.

16. A method comprising:

alternatingly charging and discharging a power storage element to generate a DC output voltage from an input voltage;

generating an error signal from the output voltage;

generating a ramp signal from the error signal;

comparing the ramp signal to a preset threshold voltage to generate a pulse signal; and

using the pulse signal to control the charging and discharging of the power storage element.

17. The method of claim 16, further comprising:

sampling the output voltage to generate a feedback signal, and

wherein generating the error signal uses the feedback signal as representative of the output voltage.

18. The method of claim 16, wherein

generating the ramp signal includes charging a ramp capacitor in accordance with the error signal.

19. The method of claim 18, wherein

charging is performed through a linear element.

20. The method of claim 18, further comprising:

shorting the ramp capacitor responsive to a clock signal.